

SAID
BY
COUNCIL
AW

forming a first layer over at least the isolation structure; and
forming a contact hole in the first layer in an area above the isolation structure, the contact hole having a width smaller than the minimum processing size of the photolithographic process.

REMARKS

Claims 1-9 and 21-40 are pending in this application. Claims 10-20 were cancelled in the Preliminary Amendment filed January 28, 1998. Each of the pending claims is believed to define an invention which is novel and unobvious over the cited art. Favorable reconsideration of this case is respectfully requested.

An ABSTRACT OF THE DISCLOSURE is submitted herewith on a separate sheet as required by the Examiner.

The specification has been objected to under 35 U.S.C. §112, first paragraph, first paragraph, as containing terms which are not clear, concise and exact.

The specification has been amended to correct all the deficiencies noted by the Examiner.

Regarding page 12, lines 16-19, it is clear from both the specification and drawings which two portions of oxide film 12 are referred to. This portion of the specification specifically mentions that the area between the two portions should not be filled with polycrystalline silicon film 13. Applicants respectfully submit that it would be apparent to one skilled in the art that this is referring to, for

example, the area lying between the two film portions 12 shown in Figure 3e. By making the thickness of polycrystalline silicon film 13 approximately one-third the thickness of layer 12, this ensures that this region is not completely filled.

Accordingly, in view of the above discussion, it is respectfully submitted that the present specification is in all aspects in compliance with 35 U.S.C. §112, first paragraph. Therefore, the withdrawal of this rejection is respectfully requested.

The present invention relates to a method for forming a semiconductor device. As recited in new claim 21, for example, the method may use a lithographic process having a determined minimum processing feature size. A semiconductor element is formed in a substrate. A conductive layer 8 is formed over the semiconductor element and the substrate. A first mask layer 12 is formed on the conductive layer 8. The first mask layer 8 is patterned to form a slit dividing the first mask layer into at least two mask portions 12. The slit preferably has a width equal in size to the minimum processing feature size and has side walls corresponding to end faces of the two mask portions. A second mask layer 13 is formed on the slit side walls, thereby reducing the width of the slit. Next, the conductive layer 8 is etched using the first, and second mask layers 12, 13. The etching separates the conductive layer 8 into at least two conductive layer portions. The at least two conductive layer portions are separated by a distance which is less than the minimum process feature size.

Claims 1-5 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,994,402 to Chiu or U.S. Patent No. 5,134,083 to Mathews.

Neither of the cited references anticipate the present invention since they fail to disclose, among other things, patterning a layer to have a hole or opening which is smaller than the minimum size achievable by a lithographic process. Column 1, lines 47-52 and column 2, lines 61-64 of Chiu, referred to in the official action, do not describe the aforementioned feature of the present invention. These portions of the reference mainly describe forming source and drain diffusion regions and contacts. There is no mention in Chiu of forming openings or holes in a conductive layer which are smaller than the minimum feature processing size, and as recited in new independent claims 21, 28, 30, 32 and 33.

Additionally, independent claim 1 has been amended to recite that the gate electrode is formed with a width which is equal to the minimum processing size achievable with lithography technique. The formation of the gate electrodes in Chiu, described in column 5, lines 20-30, makes no mention of this feature.

Matthews also fails to describe the features recited in the pending claims. Matthews describes a method for forming a CMOS integrated circuit having MOSFETs and bipolar junction transistors formed in the same silicon substrate. Columns 2 and 3 of Matthews, referred to in the Office Action, make no mention of the features recited in new claims 21-40 and in amended claim 1. Column 3, lines 9-19 of Matthews describe the formation of the gate electrodes for MOS transistors. There is no mention that the gate electrodes are formed with a minimum processing size. There is no mention in Matthews of patterning a conductive layer to have holes or openings between portions thereof which are smaller than the minimum processing size achievable by the lithographic process, as is recited in the pending claims.

Every pending claim now recites forming holes, openings, etc. in a layer which are smaller than the minimum processing site obtainable by the lithographic process used.

Anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims. See, e.g., *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985). There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. § 102. See, e.g., *Scripps Clinic and Research Foundation v. Genetech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).

In view of the above, it is clear that the cited references do not disclose each and every element of the claims as is recited by 35 U.S.C. §102(b). Therefore, the withdrawal of this rejection is respectfully requested.

Claims 6-9 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chiu of Matthews, as described above, and further in view of U.S. Patent 5,073,510 to Kwon et al.

Chiu and Matthews have been described above. Kwon et al. does not supplement the primary references to teach or suggest the present invention. Kwon et al. describes a method for forming a contact window in a semiconductor device. There is no mention in Kwon et al. of forming a gate electrode at the minimum processing size or of forming openings or holes in a conductive layer which are smaller than the minimum processing size achievable with the lithograph process.

In view of the above, it is clear that the cited references, taken alone or in

combination, do not teach or suggest the features of the present invention. Therefore, the withdrawal of this rejection is respectfully requested.

In view of the above discussion and amendments to the claims, it is respectfully submitted that all pending claims are now allowable.

Accordingly, favorable reconsideration of this case and early issuance of the Notice of Allowance are respectfully requested.

The Commissioner is hereby authorized to charge any insufficient fees or credit any overpayment associated with this application to Deposit Account No. 22-0185. A duplicate of this authorization is attached for the Finance Branch.

In the event that any further cooperation in this case is deemed to be necessary to complete its prosecution, the Examiner is urged to contact the undersigned at the telephone number listed below.

Respectfully submitted

AC Jeffrey A. Kaminski 42,700
Ezbieta Chlopecka, Reg. No. 32,767
Pollock, Vande Sande & Amernick, R.L.L.P.
1990 M Street, N.W.
Washington, D.C. 20036-3425
Telephone: 202-331-7111

Date: 3/28/00